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Extended Display Identification Data

Extended Display Identification Data (**EDID**) is a metadata format for display devices to describe their capabilities to a video source (e.g. graphics card or set-top box). The data format is defined by a standard published by the Video Electronics Standards Association (VESA).

The EDID data structure includes manufacturer name and serial number, product type, phosphor or filter type, timings supported by the display, display size, luminance data and (for digital displays only) pixel mapping data.

DisplayID is a VESA standard targeted to replace EDID and E-EDID extensions with a uniform format suited for both PC monitor and consumer electronics devices.

All CTA standards are free to everyone since May 2018.[1][2]

Contents

Background

EDID structure versions range from v1.0 to v1.4; all these define upwards-compatible 128-byte structures. Version 2.0 defined a new 256-byte structure but it has been deprecated and replaced by v1.3 which supports multiple extension blocks. HDMI versions 1.0–1.3c use EDID structure v1.3.[3]

Before Display Data Channel (DDC) and EDID were defined, there was no standard way for a graphics card to know what kind of display device it was connected to. Some VGA connectors in personal computers provided a basic form of identification by connecting one, two or three pins to ground, but this coding was not standardized.

The channel for transmitting the EDID from the display to the graphics card is usually the I²C-bus, defined in DDC2B (DDC1 used a different serial format which never gained popularity).

The EDID is often stored in the monitor in a memory device called a serial PROM (programmable read-only memory) or EEPROM (electrically erasable PROM) and is accessible via the I²C-bus at address `A0`. The EDID PROM can often be read by the host PC even if the display itself is turned off.

Many software packages can read and display the EDID information, such as read-edid[4] for Linux and DOS, PowerStrip[5] for Microsoft Windows and XFree86 for Linux and BSD unix. Mac OS X natively reads EDID information and programs such as SwitchResX[6] or

DisplayConfigX[7] can display the information as well as use it to define custom resolutions.

Enhanced EDID was introduced at the same time as E-DDC; it introduced EDID structure version 1.3 which supports multiple extensions blocks and deprecated EDID version 2.0 structure (although it can be supported as an extension). Data fields for preferred timing, range limits, and monitor name are required in E-EDID. E-EDID also supports dual GTF timings and aspect ratio change.

With the use of extensions, E-EDID string can be lengthened up to 32 KBytes.

EDID Extensions assigned by VESA

- Timing Extension (00)
- Additional Timing Data Block (CEA EDID Timing Extension) (02)
- Video Timing Block Extension (VTB-EXT) (10)
- EDID 2.0 Extension (20)
- Display Information Extension (DI-EXT) (40)
- Localized String Extension (LS-EXT) (50)
- Microdisplay Interface Extension (MI-EXT) (60)
- Display ID Extension (70)
- Display Transfer Characteristics Data Block (DTCDB) (A7, AF, BF)
- Block Map (F0)
- Display Device Data Block (DDDB) (FF)
- Extension defined by monitor manufacturer (FF): According to LS-EXT, actual contents varies from manufacturer. However, the value is later used by DDDB.

Revision history

- August 1994, DDC standard version 1 – EDID v1.0 structure.
- April 1996, EDID standard version 2 – EDID v1.1 structure.
- 1997, EDID standard version 3 – EDID structures v1.2 and v2.0

- February 2000, E-EDID Standard Release A, v1.0 – EDID structure v1.3, EDID structure v2.0 deprecated
- September 2006 – E-EDID Standard Release A, v2.0 – EDID structure v1.4

Limitations

Some graphics card drivers have historically coped poorly with the EDID, using only its standard timing descriptors rather than its Detailed Timing Descriptors (DTDs). Even in cases where the DTDs were read, the drivers are/were still often limited by the standard timing descriptor limitation that the horizontal/vertical resolutions must be evenly divisible by 8. This means that many graphics cards cannot express the native resolutions of the most common wide screen flat panel displays and liquid crystal display televisions. The number of vertical pixels is calculated from the horizontal resolution and the selected aspect ratio. To be fully expressible, the size of wide screen display must thus be a multiple of 16×9 pixels. For 1366×768 pixel Wide XGA panels the nearest resolution expressible in the EDID standard timing descriptor syntax is 1360×765 pixels, typically leading to 3 pixel thin black bars. Specifying 1368 pixels as the screen width would yield an unnatural screen height of 769.5 pixels.

Many Wide XGA panels do not advertise their native resolution in the standard timing descriptors, instead offering only a resolution of 1280×768. Some panels advertise a resolution only slightly smaller than the native, such as 1360×765. For these panels to be able to show a pixel perfect image, the EDID data must be ignored by the display driver or the driver must correctly interpret the DTD and be able to resolve resolutions whose size is not divisible by 8. Special programs are available to override the standard timing descriptors from EDID data. Even this is not always possible, as some vendors' graphics drivers (notably those of Intel) require specific registry hacks to implement custom resolutions, which can make it very difficult to use the screen's native resolution.[8]

EDID 1.4 data format

Structure, version 1.4

EDID structure, version 1.4[9][10]

Bytes	Description	
0–19	**Header information**	
0–7	Fixed header pattern: `00 FF FF FF FF FF FF 00`	
8–9	Manufacturer ID. This is a legacy Plug and Play ID assigned by Microsoft, which is a *big-endian* 16-bit value made up of three 5-bit letters: 00001, A; 00010, B; ...; 11010, Z. E.g., 24 4d, 0 01001 00010 01101, "IBM".	
	Bit 15	`0` = reserved
	Bits 14–10	First letter of manufacturer ID (byte 8, bits 6–2)
	Bits 9–5	Second letter of manufacturer ID (byte 8, bit 1 through byte 9 bit 5)
	Bits 4–0	Third letter of manufacturer ID (byte 9 bits 4–0)
10–11	Manufacturer product code. 16-bit number, little-endian.	
12–15	Serial number. 32 bits, little-endian.	
16	Week of manufacture; or FF model year flag. Week numbering is not consistent between manufacturers.	
17	Year of manufacture, or year of model, if model year flag is set. Year = datavalue + 1990.	
18	EDID version, usually `01` (for 1.3 and 1.4)	
19	EDID revision, usually `03` (for 1.3) or `04` (for 1.4)	
20–24	**Basic display parameters**	
20	Video input parameters bitmap	
	Bit 7 = 1	Digital input. If set, the following bit definitions apply:
	Bits 6–4	Bit depth: `000` = undefined `001` = 6

	010 = 8 011 = 10 100 = 12 101 = 14 110 = 16 bits per color 111 = reserved
Bits 3–0	Video interface: 0000 = undefined 0010 = HDMIa 0011 = HDMIb 0100 = MDDI 0101 = DisplayPort
Bit 7 = 0	Analog input. If clear, the following bit definitions apply:
Bits 6–5	Video white and sync levels, relative to blank: 00 = +0.7/−0.3 V 01 = +0.714/−0.286 V 10 = +1.0/−0.4 V 11 = +0.7/0 V
Bit 4	Blank-to-black setup (pedestal) expected
Bit 3	Separate sync supported
Bit 2	Composite sync (on HSync) supported
Bit 1	Sync on green supported
Bit 0	VSync pulse must be serrated when composite or sync-on-green is used.

21	Horizontal screen size, in centimetres (range 1–255). If vertical screen size is 0, landscape aspect ratio (range 1.00–3.54), datavalue = (AR×100) − 99 (example: 16:9, 79; 4:3, 34.)	
22	Vertical screen size, in centimetres. If horizontal screen size is 0, portrait aspect ratio (range 0.28–0.99), datavalue = (100/AR) − 99 (example: 9:16, 79; 3:4, 34.) If either byte is 0, screen size and aspect ratio are undefined (e.g. projector)	
23	Display gamma, factory default (range 1.00–3.54), datavalue = (gamma×100) − 100 = (gamma − 1)×100. If 225, gamma is defined by DI-EXT block.	
24	Supported features bitmap	
	Bit 7	DPMS standby supported
	Bit 6	DPMS suspend supported
	Bit 5	DPMS active-off supported
	Bits 4–3	Display type (digital): 00 = RGB 4:4:4 01 = RGB 4:4:4 + YCrCb 4:4:4 10 = RGB 4:4:4 + YCrCb 4:2:2 11 = RGB 4:4:4 + YCrCb 4:4:4 + YCrCb 4:2:2
		Display type (analog): 00 = monochrome or grayscale 01 = RGB color 10 = non-RGB color 11 = undefined
	Bit 2	Standard sRGB colour space. Bytes 25–34 must contain sRGB standard values.
	Bit 1	Preferred timing mode specified in descriptor block 1. For EDID 1.3+ the preferred timing mode is always in the first Detailed Timing Descriptor. In that case, this bit specifies whether the preferred timing mode includes native pixel format and refresh rate.

	Bit 0	Continuous timings with GTF or CVT
25–34	**Chromaticity coordinates. 10-bit CIE 1931 xy coordinates for red, green, blue, and white point**	
25	Red and green least-significant bits (2^{-9}, 2^{-10})	
	Bits 7–6	Red *x* value least-significant 2 bits
	Bits 5–4	Red *y* value least-significant 2 bits
	Bits 3–2	Green *x* value least-significant 2 bits
	Bits 1–0	Green *y* value least-significant 2 bits
26	Blue and white least-significant 2 bits	
27	Red *x* value most significant 8 bits (2^{-1}, ..., 2^{-8}). 0–255 encodes fractional 0–0.996 (255/256); 0–0.999 (1023/1024) with lsbits	
28	Red *y* value most significant 8 bits	
29–30	Green *x* and *y* value most significant 8 bits	
31–32	Blue *x* and *y* value most significant 8 bits	
33–34	Default white point *x* and *y* value most significant 8 bits	
35–37	**Established timing bitmap. Supported bitmap for (formerly) very common timing modes.**	
35	Bit 7	720×400 @ 70 Hz (VGA)
	Bit 6	720×400 @ 88 Hz (XGA)
	Bit 5	640×480 @ 60 Hz (VGA)
	Bit 4	640×480 @ 67 Hz (Apple Macintosh II)
	Bit 3	640×480 @ 72 Hz
	Bit 2	640×480 @ 75 Hz

	Bit 1	800×600 @ 56 Hz
	Bit 0	800×600 @ 60 Hz
36	Bit 7	800×600 @ 72 Hz
	Bit 6	800×600 @ 75 Hz
	Bit 5	832×624 @ 75 Hz (Apple Macintosh II)
	Bit 4	1024×768 @ 87 Hz, interlaced (1024×768i)
	Bit 3	1024×768 @ 60 Hz
	Bit 2	1024×768 @ 70 Hz
	Bit 1	1024×768 @ 75 Hz
	Bit 0	1280×1024 @ 75 Hz
37	Bit 7	1152x870 @ 75 Hz (Apple Macintosh II)
	Bits 6–0	Other manufacturer-specific display modes
38–53	**Standard timing information. Up to 8 2-byte fields describing standard display modes. Unused fields are filled with `01 01` hex. The following definitions apply in each record:**	
0	X resolution, `00` = reserved; otherwise, (datavalue + 31) × 8 (256–2288 pixels).	
1	Bits 7–6	Image aspect ratio: `00` = 16:10 `01` = 4:3 `10` = 5:4 11 = 16:9 (Versions prior to 1.3 defined `00` as 1:1.)
	Bits 5–0	Vertical frequency, datavalue + 60 (60–123 Hz)

54–71	Descriptor 1	18 byte descriptors. Detailed timing descriptors, in decreasing preference order, followed by Display descriptors
72–89	Descriptor 2	
90–107	Descriptor 3	
108–125	Descriptor 4	
126	Number of extensions to follow. 0 if no extensions.	
127	Checksum. Sum of all 128 bytes should equal 0 (mod 256).	

Detailed Timing Descriptor

EDID Detailed Timing Descriptor[9]

Bytes	Description	
0–1	Pixel clock. 00 = reserved; otherwise in 10 kHz units (0.01–655.35 MHz, little-endian).	
2	Horizontal active pixels 8 lsbits (0–4095)	
3	Horizontal blanking pixels 8 lsbits (0–4095) End of active to start of next active.	
4	Bits 7–4	Horizontal active pixels 4 msbits
	Bits 3–0	Horizontal blanking pixels 4 msbits
5	Vertical active lines 8 lsbits (0–4095)	
6	Vertical blanking lines 8 lsbits (0–4095)	
7	Bits 7–4	Vertical active lines 4 msbits
	Bits 3–0	Vertical blanking lines 4 msbits
8	Horizontal front porch (sync offset) pixels 8 lsbits (0–1023) From blanking start	
9	Horizontal sync pulse width pixels 8 lsbits (0–1023)	
10	Bits 7–4	Vertical front porch (sync offset) lines 4 lsbits (0–63)
	Bits 3–0	Vertical sync pulse width lines 4 lsbits (0–63)
11	Bits 7–6	Horizontal front porch (sync offset) pixels 2 msbits
	Bits 5–4	Horizontal sync pulse width pixels 2 msbits
	Bits 3–2	Vertical front porch (sync offset) lines 2 msbits
	Bits 1–0	Vertical sync pulse width lines 2 msbits
12	Horizontal image size, mm, 8 lsbits (0–4095 mm, 161 in)	
13	Vertical image size, mm, 8 lsbits (0–4095 mm, 161 in)	
14	Bits 7–4	Horizontal image size, mm, 4 msbits

	Bits 3–0	Vertical image size, mm, 4 msbits
15	Horizontal border pixels (one side; total is twice this)	
16	Vertical border lines (one side; total is twice this)	
17	Features bitmap	
	Bit 7	Interlaced
	Bits 6–5	Stereo mode (combine bits 6–5 with bit 0): 00 0 = none, bit 0 is reserved; 01 0 = field sequential, right during stereo sync; 10 0 = field sequential, left during stereo sync; 01 1 = 2-way interleaved, right image on even lines; 10 1 = 2-way interleaved, left image on even lines; 11 0 = 4-way interleaved; 11 1 = side-by-side interleaved.
	Bit 4 = 0	**Analog sync.** **If set, the following bit definitions apply:**
	Bit 3	Sync type: 0 = analog composite; 1 = bipolar analog composite.
	Bit 2	VSync serration (HSync during VSync)
	Bit 1	Sync on red and blue lines additionally to green
	Bits 4–3 = 10	**Digital sync., composite (on HSync).** **If set, the following bit definitions apply:**
	Bit 2	Vertical sync polarity

	0 = negative; 1 = positive.
Bit 1	0 = reserved
Bits 4–3 = 11	**Digital sync., separate** **If set, the following bit definitions apply:**
Bit 2	VSync serration (HSync during VSync)
Bit 1	Horizontal sync polarity: 0 = negative; 1 = positive.
Bit 0	**Stereo mode (combines with bits 6-5)**

When used for another descriptor, the pixel clock and some other bytes are set to 0:

Display Descriptors

EDID Display Descriptors[9]

Bytes	Description
0–1	0 = Display Descriptor (cf. Detailed Timing Descriptor).
2	0 = reserved
3	Descriptor type. FA–FF currently defined. 00–0F reserved for vendors.
4	0 = reserved, except for Display Range Limits Descriptor.
5–17	Defined by descriptor type. If text, code page 437 text, terminated (if less than 13 bytes) with LF and padded with SP.

Currently defined descriptor types are:

- FF: Display serial number (ASCII text)
- FE: Unspecified text (ASCII text)
- FD: Display range limits. 6- or 13-byte (with additional timing) binary descriptor.
- FC: Display name (ASCII text).
- FB: Additional white point data. 2× 5-byte descriptors, padded with `0A 20 20`.
- FA: Additional standard timing identifiers. 6× 2-byte descriptors, padded with `0A`.
- F9: Display Color Management (DCM).
- F8: CVT 3-Byte Timing Codes.
- F7: Additional standard timing 3.
- 10: Dummy identifier.
- 00–0F: Manufacturer reserved descriptors.

Display Range Limits

Descriptor

EDID Display Range Limits Descriptor[9]

Bytes	Description	
0–1	`00 00` = Display Descriptor	
2	`00` = reserved	
3	`FD` = Display Range Limits Descriptor	
4	Offsets for display range limits	
	Bits 7–4	`00` = reserved
	Bits 3–2	Horizontal rate offsets: `00` = none; `10` = +255 kHz for max. rate; `11` = +255 kHz for max. and min. rates.
	Bits 1–0	Vertical rate offsets: `00` = none; `10` = +255 Hz for max. rate; `11` = +255 Hz for max. and min. rates.
5	Minimum	vertical field rate (1–255 Hz; 256–512 Hz, if offset).
6	Maximum	
7	Minimum	horizontal line rate (1–255 kHz; 256–512 kHz, if offset).
8	Maximum	
9	Maximum pixel clock rate, rounded up to 10 MHz multiple (10–2550 MHz).	
10	Extended timing information type:	

	00 = Default GTF (when basic display parameters byte 24, bit 0 is set). 01 = No timing information. 02 = Secondary GTF supported, parameters as follows. 04 = CVT (when basic display parameters byte 24, bit 0 is set), parameters as follows.
11–17	Video timing parameters (if byte 10 is 00 or 01, padded with 0A 20 20 20 20 20 20).

With GTF secondary curve

EDID Display Range Limits with GTF Secondary curve[9]

Bytes	Description
10	02
11	00 = reserved
12	Start frequency for secondary curve, divided by 2 kHz (0–510 kHz)
13	GTF *C* value, multiplied by 2 (0–127.5)
14–15	GTF *M* value (0–65535, little-endian)
16	GTF *K* value (0–255)
17	GTF *J* value, multiplied by 2 (0–127.5)

With CVT support

EDID Display Range Limits with CVT support[9]

Bytes	Description	
10	04	
11	Bits 7–4	CVT major version (1–15)
	Bits 3–0	CVT minor version (0–15)
12	Bits 7–2	Additional clock precision in 0.25 MHz increments (to be subtracted from byte 9 maximum pixel clock rate)
	Bits 1–0	Maximum active pixels per line, 2-bit msb
13	Maximum active pixels per line, 8-bit lsb (no limit if 0)	
14	Aspect ratio bitmap	
	Bit 7	4:3
	Bit 6	16:9
	Bit 5	16:10
	Bit 4	5:4
	Bit 3	15:9
	Bits 2–0	000 = reserved
15	Bits 7–5	Aspect ratio preference: 000 = 4:3 001 = 16:9 010 = 16:10 011 = 5:4 100 = 15:9
	Bit 4	CVT-RB reduced blanking (preferred)

	Bit 3	CVT standard blanking
	Bits 2–0	`000` = reserved
16	Scaling support bitmap	
	Bit 7	Horizontal shrink
	Bit 6	Horizontal stretch
	Bit 5	Vertical shrink
	Bit 4	Vertical stretch
	Bits 3–0	`0000` = reserved
17	Preferred vertical refresh rate (1–255)	

Additional white point descriptor

EDID additional white point descriptor[9]

Bytes	Description	
0–4	`00 00 00` FB `00`	
5	White point index number (1–255). Usually 1; 0 indicates descriptor not used.	
6	White point CIE xy coordinates least-significant bits (like EDID byte 26)	
	Bits 7–4	`000` = reserved
	Bits 3–2	White point *x* value least-significant 2 bits
	Bits 1–0	White point *y* value least-significant 2 bits
7	White point *x* value most significant 8 bits (like EDID byte 27)	
8	White point *y* value most significant 8 bits (like EDID byte 28)	
9	datavalue = (gamma − 1)×100 (1.0–3.54, like EDID byte 23)	
10–14	Second descriptor, like above. Index number usually 2.	
15–17	Unused, padded with `0A 20 20`.	

Color management data descriptor

EDID color management data descriptor[9]

Bytes	Description
0–4	`00 00 00 F9 00`
5	Version: `03`
6	Red a_3 lsb
7	Red a_3 msb
8	Red a_2 lsb
9	Red a_2 msb
10	Green a_3 lsb
11	Green a_3 msb
12	Green a_2 lsb
13	Green a_2 msb
14	Blue a_3 lsb
15	Blue a_3 msb
16	Blue a_2 lsb
17	Blue a_2 msb

CVT 3-byte timing codes descriptor

EDID CVT 3-byte timing codes descriptor[9]

Bytes	Description	
0–4	`00 00 00` F8 `00`	
5	Version: `01`	
6-8	**CVT timing descriptor #1**	
6	Addressable lines 8-bit lsb	
7	Bits 7–4	Addressable lines 4-bit msb
	Bits 3–2	Aspect ratio: `00` = 4:3 `01` = 16:9 `10` = 16:10 `11` = 15:9
	Bits 1–0	`00` = reserved
8	Bit 7	`0` = reserved
	Bits 6–5	Preferred vertical rate: `00`: 50 Hz `01`: 60 Hz `10`: 75 Hz `11`: 85 Hz
	Vertical rate bitmap	
	Bit 4	50 Hz CVT
	Bit 3	60 Hz CVT

	Bit 2	75 Hz CVT
	Bit 1	85 Hz CVT
	Bit 0	60 Hz CVT reduced blanking
9–11	**CVT timing descriptor #2**	
12–14	**CVT timing descriptor #3**	
15–17	**CVT timing descriptor #4**	

Additional standard timings

EDID Additional standard timings 3[9]

Bytes	Description		
0–4	`00 00 00 F7 00`		
5	Version: `10`		
6	Bit 7	640×350	@ 85 Hz
	Bit 6	640×400	
	Bit 5	720×400	
	Bit 4	640×480	
	Bit 3	848×480	@ 60 Hz
	Bit 2	800×600	@ 85 Hz
	Bit 1	1024×768	
	Bit 0	1152×864	
7	Bit 7	1280×768	@ 60 Hz (CVT-RB)
	Bit 6		@ 60 Hz
	Bit 5		@ 75 Hz
	Bit 4		@ 85 Hz
	Bit 3	1280×960	@ 60 Hz
	Bit 2		@ 85 Hz
	Bit 1	1280×1024	@ 60 Hz
	Bit 0		@ 85 Hz
8	Bit 7	1360×768	@ 60 Hz (CVT-RB)
	Bit 6	1280×768	@ 60 Hz

	Bit 5	1440×900	@ 60 Hz (CVT-RB)
	Bit 4		@ 75 Hz
	Bit 3		@ 85 Hz
	Bit 2	1440×1050	@ 60 Hz (CVT-RB)
	Bit 1		@ 60 Hz
	Bit 0		@ 75 Hz
9	Bit 7		@ 85 Hz
	Bit 6	1680×1050	@ 60 Hz (CVT-RB)
	Bit 5		@ 60 Hz
	Bit 4		@ 75 Hz
	Bit 3		@ 85 Hz
	Bit 2	1600×1200	@ 60 Hz
	Bit 1		@ 65 Hz
	Bit 0		@ 70 Hz
10	Bit 7		@ 75 Hz
	Bit 6		@ 85 Hz
	Bit 5	1792×1344	@ 60 Hz
	Bit 4		@ 75 Hz
	Bit 3	1856×1392	@ 60 Hz
	Bit 2		@ 75 Hz
	Bit 1	1920×1200	@ 60 Hz (CVT-RB)

	Bit 0		@ 60 Hz
11	Bit 7		@ 75 Hz
	Bit 6		@ 85 Hz
	Bit 5	1920×1440	@ 60 Hz
	Bit 4		@ 75 Hz
	Bits 3–0	0000 = reserved	
12–17	Unused, must be 0.		

EIA/CEA-861 extension block

The CEA EDID Timing Extension was first introduced in EIA/CEA-861, and has since been updated several times, most notably with the −861B revision (which was version 3 of the extension, adding Short Video Descriptors and advanced audio capability/configuration information), −861D (published in July 2006 and containing updates to the audio segments), −861E, and −861F which was published on June 4, 2013.[11] According to Brian Markwalter, senior vice president, research and standards, CEA, −861F "includes a number of noteworthy enhancements, including support for several new Ultra HD and widescreen video formats and additional colorimetry schemes."[12]

The most recent version, CTA-861-G,[13] originally published in November 2016, was made available for free in November 2017 after some necessary changes due to a trademark complaint.

Version 1 (as defined in −861) allowed the specification of video timings only through the use of 18-byte Detailed Timing Descriptors (DTD) (as detailed in EDID 1.3 data format above). In all cases, the "preferred" timing should be the first DTD listed in a CEA EDID Timing Extension.

Version 2 (as defined in −861A) added the capability to designate a number of DTDs as "native" and also included some "basic discovery" functionality for whether the display device contains support for "basic audio", YCbCr pixel formats, and underscan.

Version 3 (from the −861B spec) allows two different ways to specify the timings of available digital TV formats: As in Version 1 & 2 by the use of 18-byte DTDs, or by the use of the Short Video Descriptor (SVD) (see below). HDMI 1.0−1.3c uses this version.

Version 3 also includes four new optional types of data blocks: Video Data Blocks containing the aforementioned Short Video Descriptor (SVD), Audio Data Blocks containing Short Audio Descriptors (SAD), Speaker Allocation Data Blocks containing information about the speaker configuration of the display device, and Vendor Specific Data Blocks which can contain information specific to a given vendor's use.

CEA EDID Timing Extension data format - Version 3

Byte	Description	
0	Extension tag (which kind of extension block this is); `02` for CEA EDID	
1	Revision number (version number); `03` for version 3	
2	Byte number (decimal) within this block where the 18-byte DTDs begin. If no non-DTD data is present in this extension block, the value should be set to `04` (the byte after next). If set to `00`, there are no DTDs present in this block and no non-DTD data.	
3	Number of Native DTDs present, other version 2+ information	
	Bit 7	1 if display supports underscan, `0` if not
	Bit 6	1 if display supports basic audio, `0` if not
	Bit 5	1 if display supports YCbCr 4:4:4, `0` if not
	Bit 4	1 if display supports YCbCr 4:2:2, `0` if not
	Bit 3–0	Total number of native formats in the DTDs included in this block
4–126	Data Block Collection, starting at byte 4, ending immediately before the byte specified in byte 2. If byte 2 is `04`, the collection is of zero length (i.e. not present).	
	18-byte descriptors, starting at the byte specified in byte 2. Consecutive descriptors are present while the bytes 0–1 of each are not `00 00`.	
	Padding, from the absence of an 18-byte descriptor onwards; must be `00`.	
127	Checksum. Value such that the sum of all 128 bytes is `00`.	

The Data Block Collection contains one or more data blocks detailing video, audio, and speaker placement information about the display.

The blocks can be placed in any order, and the initial byte of each block defines both its type and its length:

Data block header

Byte	Description	
0	Bit 7–5	Block Type Tag ▪ `001` 1: audio ▪ `010` 2: video ▪ `011` 3: vendor specific ▪ `100` 4: speaker allocation ▪ else reserved
	Bit 4–0	Total number of bytes in this block following this byte.

Once one data block has ended, the next byte is assumed to be the beginning of the next data block. This is the case until the byte (designated in byte 2, above) where the DTDs are known to begin.

Audio Data Blocks contain one or more 3-byte Short Audio Descriptors (SADs). Each SAD details audio format, channel number, and bitrate/resolution capabilities of the display as follows:

Short Audio Descriptor

Byte	Description	
0	Data block header	
1	Format and number of channels:	
	Bit 7	Reserved, `0`
	Bit 6–3	Audio format code ■ `0000` 0: reserved ■ `0001` 1: Linear Pulse Code Modulation (LPCM) ■ `0010` 2: AC-3 ■ `0011` 3: MPEG-1 (Layers 1 and 2) ■ `0100` 4: MP3 ■ `0101` 5: MPEG-2 ■ `0110` 6: AAC ■ `0111` 7: DTS ■ `1000` 8: ATRAC ■ `1001` 9: 1-bit audio, Super Audio CD ■ `1010` 10: DD+ ■ `1011` 11: DTS-HD ■ `1100` 12: MLP/Dolby TrueHD ■ `1101` 13: DST Audio ■ `1110` 14: Microsoft WMA Pro ■ `1111` 15: reserved
	Bit 2–0	Number of channels minus 1 ■ `000` 1 channel ■ `001` 2 channels ■ `010` 3 channels

		▪ 011 4 channels ▪ 100 5 channels ▪ 101 6 channels ▪ 110 7 channels ▪ 111 8 channels
2	Sampling frequencies (kHz) supported:	
	Bit 7	Reserved, 0
	Bit 6	192
	Bit 5	176
	Bit 4	96
	Bit 3	88
	Bit 2	48
	Bit 1	44.1
	Bit 0	32
3	Bitrate / format dependent:	
	For codec 1, LPCM:	
	Bits 7–3	Reserved
	Bit 2	24-bit depth
	Bit 1	20-bit depth
	Bit 0	16-bit depth
	For audio format codecs 2–8, the maximum supported bitrate in bit/s, divided by 8000.	

Video Data Blocks will contain one or more 1-byte Short Video Descriptors (SVDs).

Byte	Description	
0	Data block header	
1	Bit 7	1 to designate that this should be considered a "native" resolution, 0 for non-native
	Bit 6–0	Index value to a table of standard resolutions/timings from EIA/CEA-861:

EIA/CEA-861 standard resolutions and timings

VIC	Short name	Aspect ratio		Clock			Active		Total		Field rate (Hz)
		DAR	PAR	Pixel (MHz)	V (Hz)	H (kHz)	H	V	H	V	
1	DMT0659	4:3	1:1	25.175	59.94	31.469	640	480	800	525	60
2	480p	4:3	8:9	27	59.94	31.469	720	480	858	525	60
3	480pH	16:9	32:27	27	59.94	31.469	720	480	858	525	60
4	720p	16:9	1:1	74.25	60	45.0	1280	720	1650	750	60
5	1080i	16:9	1:1	74.25	60	33.75	1920	540	2200	562.5	60
6	480i	4:3	8:9	27	59.94	15.734	1440	240	1716	262.5	60
7	480iH	16:9	32:27	27	59.94	15.734	1440	240	1716	262.5	60
8	240p	4:3	4:9	27	59.826	15.734	1440	240	1716	262.5	60
9	240pH	16:9	16:27	27	59.826	15.734	1440	240	1716	262.5	60
10	480i4x	4:3	2:9-20:9	54	59.94	15.734	2880	240	3432	262.5	60
11	480i4xH	16:9	8:27-80:27	54	59.94	15.734	2880	240	3432	262.5	60
12	240p4x	4:3	1:9-10:9	54	60	15.734	2880	240	3432	262.5	60
13	240p4xH	16:9	4:27-40:27	54	60	15.734	2880	240	3432	262.5	60
14	480p2x	4:3	4:9, 8:9	54	59.94	31.469	1440	480	1716	525	60
15	480p2xH	16:9	16:27, 32:27	54	59.94	31.469	1440	480	1716	525	60
16	1080p	16:9	1:1	148.5	60	67.5	1920	1080	2200	1125	60
17	576p	4:3	16:15	27	50	31.25	720	576	864	625	50
18	576pH	16:9	64:45	27	50	31.25	720	576	864	625	50

VIC	Short name	Aspect ratio		Clock			Active		Total		Field rate (Hz)
		DAR	PAR	Pixel (MHz)	V (Hz)	H (kHz)	H	V	H	V	
19	720p50	16:9	1:1	74.25	50	37.5	1280	720	1980	750	50
20	1080i25	16:9	1:1	74.25	50	28.125	1920	540	2640	562.5	50
21	576i	4:3	16:15	27	50	15.625	1440	288	1728	312.5	50
22	576iH	16:9	64:45	27	50	15.625	1440	288	1728	312.5	50
23	288p	4:3	8:15	27	50	15.625	1440	288	1728	313	50
24	288pH	16:9	32:45	27	50	15.625	1440	288	1728	313	50
25	576i4x	4:3	2:15-20:15	54	50	15.625	2880	288	3456	312.5	50
26	576i4xH	16:9	16:45-160:45	54	50	15.625	2880	288	3456	312.5	50
27	288p4x	4:3	1:15-10:15	54	50	15.625	2880	288	3456	313	50
28	288p4xH	16:9	8:45-80:45	54	50	15.625	2880	288	3456	313	50
29	576p2x	4:3	8:15, 16:15	54	50	31.25	1440	576	1728	625	50
30	576p2xH	16:9	32:45, 64:45	54	50	31.25	1440	576	1728	625	50
31	1080p50	16:9	1:1	148.5	50	56.25	1920	1080	2640	1125	50
32	1080p24	16:9	1:1	74.25	23.98/24	27	1920	1080	2750	1125	Low
33	1080p25	16:9	1:1	74.25	25	28.125	1920	1080	2640	1125	Low
34	1080p30	16:9	1:1	74.25	29.97/30	33.75	1920	1080	2200	1125	Low
35	480p4x	4:3	2:9, 4:9, 8:9	108	59.94	31.469	2880	240	3432	262.5	60
36	480p4xH	16:9	8:27, 16:27, 32:27	108	59.94	31.469	2880	240	3432	262.5	60

VIC	Short name	Aspect ratio		Clock			Active		Total		Field rate (Hz)
		DAR	PAR	Pixel (MHz)	V (Hz)	H (kHz)	H	V	H	V	
37	576p4x	4:3	4:15, 8:15, 16:15	108	50	31.25	2880	576	3456	625	50
38	576p4xH	16:9	16:45, 32:45, 64:45	108	50	31.25	2880	576	3456	625	50
39	1080i25	16:9	1:1	72	50	31.25	1920	540	2304	625	50
40	1080i50	16:9	1:1	148.5	100	56.25	1920	540	2640	562.5	100
41	720p100	16:9	1:1	148.5	100	45.0	1280	720	1980	750	100
42	576p100	4:3	16:15	54	100	62.5	720	576	864	625	100
43	576p100H	16:9	64:45	54	100	62.5	720	576	864	625	100
44	576i50	4:3	16:15	54	100	31.25	1440	576	1728	625	100
45	576i50H	16:9	64:45	54	100	31.25	1440	576	1728	625	100
46	1080i60	16:9	1:1	148.5	119.88/120	67.5	1920	540	2200	562.5	120
47	720p120	16:9	1:1	148.5	119.88/120	90.0	1280	720	1650	750	120
48	480p119	4:3	8:9	54	119.88/120	62.937	720	576	858	525	120
49	480p119H	16:9	32:27	54	119.88/120	62.937	720	576	858	525	120
50	480i59	4:3	16:15	54	119.88/120	31.469	1440	576	1716	525	120
51	480i59H	16:9	64:45	54	119.88/120	31.469	1440	576	1716	525	120
52	576p200	4:3	16:15	108	200	125.0	720	576	864	625	200
53	576p200H	16:9	64:45	108	200	125.0	720	576	864	625	200
54	576i100	4:3	16:15	108	200	62.5	1440	288	1728	312.5	200

VIC	Short name	Aspect ratio		Clock			Active		Total		Field rate (Hz)
		DAR	PAR	Pixel (MHz)	V (Hz)	H (kHz)	H	V	H	V	
55	576i100H	16:9	64:45	108	200	62.5	1440	288	1728	312.5	200
56	480p239	4:3	8:9	108	239.76	125.874	720	480	858	525	240
57	480p239H	16:9	32:27	108	239.76	125.874	720	480	858	525	240
58	480i119	4:3	8:9	108	239.76	62.937	1440	240	1716	262.5	240
59	480i119H	16:9	32:27	108	239.76	62.937	1440	240	1716	262.5	240
60	720p24	16:9	1:1	59.4	23.98/24	18.0	1280	720	3300	750	Low
61	720p25	16:9	1:1	74.25	25	18.75	1280	720	3960	750	Low
62	720p30	16:9	1:1	74.25	29.97/30	22.5	1280	720	3300	750	Low
63	1080p120	16:9	1:1	297	119.88/120	135.0	1920	1080	2200	1125	120
64	1080p100	16:9	1:1	297	100	112.5	1920	1080	2640	1125	100
65	720p24	64:27	4:3	59.4	23.98/24	18.0	1280	720	3300	750	Low
66	720p25	64:27	4:3	74.25	25	18.75	1280	720	3960	750	Low
67	720p30	64:27	4:3	74.25	29.97/30	22.5	1280	720	3300	750	Low
68	720p50	64:27	4:3	74.25	50	37.5	1280	720	1980	750	50
69	720p	64:27	4:3	74.25	60	45.0	1650	750	1650	750	60
70	720p100	64:27	4:3	148.5	100	75.0	1280	720	1980	750	100
71	720p120	64:27	4:3	148.5	119.88/120	90.0	1280	720	1650	750	120
72	1080p24	64:27	4:3	74.25	23.98/24	27	1920	1080	2750	1125	Low
73	1080p25	64:27	4:3	74.25	25	28.125	1920	1080	2640	1125	Low

VIC	Short name	Aspect ratio		Clock			Active		Total		Field rate (Hz)
		DAR	PAR	Pixel (MHz)	V (Hz)	H (kHz)	H	V	H	V	
74	1080p30	64:27	4:3	74.25	29.97/30	33.75	1920	1080	2500	1125	Low
75	1080p50	64:27	4:3	148.5	50	56.25	1920	1080	2640	1125	50
76	1080p	64:27	4:3	148.5	60	67.5	1920	1080	2200	1125	60
77	1080p100	64:27	4:3	297.0	100	112.5	1920	1080	2640	1125	100
78	1080p120	64:27	4:3	297.0	119.88/120	135.0	1920	1080	2200	1125	120
79	720p2x24	64:27	64:63	59.4	23.98/24	18.0	1680	720	3300	750	Low
80	720p2x25	64:27	64:63	59.4	25	18.75	1680	720	3168	750	Low
81	720p2x30	64:27	64:63	59.4	29.97/30	22.5	1680	720	2640	750	Low
82	720p2x50	64:27	64:63	82.5	50	37.5	1680	720	2200	750	50
83	720p2x	64:27	64:63	99	60	45.0	1680	720	2200	750	60
84	720p2x100	64:27	64:63	165	100	82.5	1680	720	2000	825	100
85	720p2x120	64:27	64:63	198	119.88/120	99.0	1680	720	2000	825	120
86	1080p2x24	64:27	1:1	99	23.98/24	26.4	2560	1080	3750	1100	Low
87	1080p2x25	64:27	1:1	90	25	28.125	2560	1080	3200	1125	Low
88	1080p2x30	64:27	1:1	118.8	29.97/30	33.75	2560	1080	3520	1125	Low
89	1080p2x50	64:27	1:1	185.625	50	56.25	2560	1080	3000	1125	50
90	1080p2x	64:27	1:1	198	60	66.0	2560	1080	3000	1100	60
91	1080p2x100	64:27	1:1	371.25	100	125.0	2560	1080	2970	1250	100
92	1080p2x120	64:27	1:1	495	119.88/120	150.0	2560	1080	3300	1250	120

VIC	Short name	Aspect ratio		Clock			Active		Total		Field rate (Hz)
		DAR	PAR	Pixel (MHz)	V (Hz)	H (kHz)	H	V	H	V	
93	2160p24	16:9	1:1	297	23.98/24	54	3840	2160	5500	2250	Low
94	2160p25	16:9	1:1	297	25	56.25	3840	2160	5280	2250	Low
95	2160p30	16:9	1:1	297	29.97/30	67.5	3840	2160	4400	2250	Low
96	2160p50	16:9	1:1	594	50	112.5	3840	2160	5280	2250	50
97	2160p60	16:9	1:1	594	60	135.0	3840	2160	4400	2250	60
98	2160p24	256:135	1:1	297	23.98/24	67.5	4096	2160	5500	2250	Low
99	2160p25	256:135	1:1	297	25	112.5	4096	2160	5280	2250	Low
100	2160p30	256:135	1:1	297	29.97/30	135.0	4096	2160	4400	2250	Low
101	2160p50	256:135	1:1	594	50	112.5	4096	2160	5280	2250	50
102	2160p	256:135	1:1	594	60	135.0	4096	2160	4400	2250	60
103	2160p24	64:27	4:3	297	23.98/24	67.5	3840	2160	5500	2250	Low
104	2160p25	64:27	4:3	297	25	112.5	3840	2160	5280	2250	Low
105	2160p30	64:27	4:3	297	29.97/30	135.0	3840	2160	4400	2250	Low
106	2160p50	64:27	4:3	594	50	112.5	3840	2160	5280	2250	50
107	2160p	64:27	4:3	594	60	135.0	3840	2160	4400	2250	60
108	720p48	16:9	1:1	90	47.96/48	36.0	1280	720	2500	750	Low
109	720p48	64:27	4:3	90	47.96/48	36.0	1280	720	2500	750	Low
110	720p2x48	64:27	64:63	99	47.96/48	36.0	1680	720	2750	825	Low
111	1080p48	16:9	1:1	148.5	47.96/48	54	1920	1080	2750	1125	Low

VIC	Short name	Aspect ratio		Clock			Active		Total		Field rate (Hz)
		DAR	PAR	Pixel (MHz)	V (Hz)	H (kHz)	H	V	H	V	
112	1080p48	64:27	4:3	148.5	47.96/48	54	1920	1080	2750	1125	Low
113	1080p2x48	64:27	1:1	198	47.96/48	52.8	2560	1080	3750	1100	Low
114	2160p48	16:9	1:1	594	47.96/48	108	3840	2160	5500	2250	Low
115	2160p48	256:135	1:1	594	47.96/48	108	4096	2160	5500	2250	Low
116	2160p48	64:27	4:3	594	47.96/48	108	3840	2160	5500	2250	Low
117	2160p100	16:9	1:1	1188	100	225.0	3840	2160	5280	2250	100
118	2160p120	16:9	1:1	1188	119.88/120	270.0	3840	2160	4400	2250	120
119	2160p100	64:27	4:3	1188	100	225.0	3840	2160	5280	2250	100
120	2160p120	64:27	4:3	1188	119.88/120	270.0	3840	2160	4400	2250	120
121	2160p2x24	64:27	1:1	396	23.98/24	52.8	5120	2160	7500	2200	Low
122	2160p2x25	64:27	1:1	396	25	55.0	5120	2160	7200	2200	Low
123	2160p2x30	64:27	1:1	396	29.97/30	66.0	5120	2160	6000	2200	Low
124	2160p2x48	64:27	1:1	742.5	47.96/48	118.8	5120	2160	6250	2450	Low
125	2160p2x50	64:27	1:1	742.5	50	112.5	5120	2160	6600	2250	50
126	2160p2x	64:27	1:1	742.5	60	135.0	5120	2160	5500	2250	60
127	2160p2x100	64:27	1:1	1485	100	225.0	5120	2160	6600	2250	100
128—192	reserved, value range is used in SVD to indicate native timing for numbers 1—64.										
193	2160p2x120	64:27	1:1	1485.0	119.88/120	270	5120	2160	5500	2250	120
194	4320p24	16:9	1:1	1188.0	23.98/24	108	7680	4320	11000	4500	Low

VIC	Short name	Aspect ratio		Clock			Active		Total		Field rate (Hz)
		DAR	PAR	Pixel (MHz)	V (Hz)	H (kHz)	H	V	H	V	
195	4320p25	16:9	1:1	1188.0	25	110	7680	4320	10800	4400	Low
196	4320p30	16:9	1:1	1188.0	29.97/30	132	7680	4320	9000	4400	Low
197	4320p48	16:9	1:1	2376.0	47.96/48	216	7680	4320	11000	4500	Low
198	4320p50	16:9	1:1	2376.0	50	220	7680	4320	10800	4400	50
199	4320p	16:9	1:1	2376.0	60	264	7680	4320	9000	4400	60
200	4320p100	16:9	1:1	4752.0	100	450	7680	4320	10560	4500	100
201	4320p120	16:9	1:1	4752.0	119.88/120	540	7680	4320	8800	4500	120
202	4320p24	64:27	4:3	1188.0	23.98/24	108	7680	4320	11000	4500	Low
203	4320p25	64:27	4:3	1188.0	25	110	7680	4320	10800	4400	Low
204	4320p30	64:27	4:3	1188.0	29.97/30	132	7680	4320	9000	4400	Low
205	4320p48	64:27	4:3	2376.0	47.96/48	216	7680	4320	11000	4500	Low
206	4320p50	64:27	4:3	2376.0	50	220	7680	4320	10800	4400	50
207	4320p	64:27	4:3	2376.0	60	264	7680	4320	9000	4400	60
208	4320p100	64:27	4:3	4752.0	100	450	7680	4320	10560	4500	100
209	4320p120	64:27	4:3	4752.0	119.88/120	540	7680	4320	8800	4500	120
210	4320p2x24	64:27	1:1	1485.0	23.98/24	118.8	10240	4320	12500	4950	Low
211	4320p2x25	64:27	1:1	1485.0	25	110	10240	4320	13500	4400	Low
212	4320p2x30	64:27	1:1	1485.0	29.97/30	135	10240	4320	11000	4500	Low
213	4320p2x48	64:27	1:1	2970.0	47.96/48	237.6	10240	4320	12500	4950	Low

VIC	Short name	Aspect ratio		Clock			Active		Total		Field rate (Hz)
		DAR	PAR	Pixel (MHz)	V (Hz)	H (kHz)	H	V	H	V	
214	4320p2x50	64:27	1:1	2970.0	50	220	10240	4320	13500	4400	50
215	4320p2x	64:27	1:1	2970.0	60	270	10240	4320	11000	4400	60
216	4320p2x100	64:27	1:1	5940.0	100	450	10240	4320	13200	4500	100
217	4320p2x120	64:27	1:1	5940.0	119.88/120	540	10240	4320	11000	4500	120
218	2160p100	256:135	1:1	1188.0	100	225	4096	2160	5280	2250	100
219	2160p120	256:135	1:1	1188.0	119.88/120	270	4096	2160	4400	2250	120

Notes: Parentheses indicate instances where pixels are repeated to meet the minimum speed requirements of the interface. For example, in the 720x240p case, the pixels on each line are double-clocked. In the (2880)x480i case, the number of pixels on each line, and thus the number of times that they are repeated, is variable, and is sent to the DTV monitor by the source device.

Increased Hactive expressions include “2x” and “4x” indicate two and four times the reference resolution, respectively.

Video modes with vertical refresh frequency being a multiple of 6 Hz (i.e. 24, 30, 60, 120, and 240 Hz) are considered to be the same timing as equivalent NTSC modes where vertical refresh is adjusted by a factor of 1000/1001. As VESA DMT specifies 0.5% pixel clock tolerance, which 5 times more than the required change, pixel clocks can be adjusted to maintain NTSC compatibility; typically, 240p, 480p, and 480i modes are adjusted, while 576p, 576i and HDTV formats are not.

- The EIA/CEA-861 and 861-A standards included only numbers 1–7 and numbers 17–22 (only in -A) above (but not as short video descriptors which were introduced in EIA/CEA-861-B) and are considered primary video format timings.
- The EIA/CEA-861-B standard has the first 34 short video descriptors above. It is used by HDMI 1.0–1.2a.
- The EIA/CEA-861-C and -D standards have the first 59 short video descriptors above. EIA/CEA-861-D is used by HDMI 1.3–1.3c.
- The EIA/CEA-861-E standard has the first 64 short video descriptors above. It is used by HDMI 1.4–1.4b.

- The CTA-861-F standard has the first 107 short video descriptors above. It is used by HDMI 2.0–2.0b.
- The CTA-861-G standard has the full list of 154 (1–127, 193–219) short video descriptors above. It is used by HDMI 2.1.

A **Vendor Specific Data Block** (if any) contains as its first three bytes the vendor's IEEE 24-bit registration number,[14] least significant byte first. The remainder of the Vendor Specific Data Block is the "data payload", which can be anything the vendor considers worthy of inclusion in this EDID extension block. For example, IEEE registration number `00 0C 03` means this is a "HDMI Licensing, LLC" specific data block (contains HDMI 1.4 info), `C4-5D-D8` means this is a "HDMI Forum" specific data block (contains HDMI 2.0 info), `00 D0 46` means this is "DOLBY LABORATORIES, INC." (contains Dolby Vision info) and `90 84 8b` is "HDR10+ Technologies, LLC" (contains HDR10+ info as part of HDMI 2.1 Amendment A1 standard[15]). It starts with a two byte source physical address, least significant byte first. The source physical address provides the CEC physical address for upstream CEC devices. HDMI 1.3a specifies some requirements for the data payload.

Vendor Specific Data Block for "HDMI Licensing LLC"

Byte	Description	
0	Data block header	
1–3	IEEE Registration Identifier (little endian)	
4–5	Components of Source Physical Address[16]	
6	(optional) 1, supported; 0, unsupported:	
	Bit 7	A function that needs info from ACP or ISRC packets
	Bit 6	16-bit-per-channel deep color (48-bit)
	Bit 5	12-bit-per-channel deep color (36-bit)
	Bit 4	10-bit-per-channel deep color (30-bit)
	Bit 3	4:4:4 in deep color modes
	Bit 2	Reserved, 0
	Bit 1	Reserved, 0
	Bit 0	DVI Dual Link Operation
7	(optional) Maximum TMDS frequency. 0, unspecified; else, Max_TMDS_Frequency / 5 MHz	
8	(optional) Latency fields indicators 1, present; 0, absent:	
	Bit 7	Latency fields
	Bit 6	Interlaced latency fields. Absent if latency fields are absent.
	Bits 5–0	Reserved, 0
9	Video latency	optional; if indicated, value = 1 + ms/2 with a max. of 251 meaning 500 ms
10	Audio latency (video delay for progressive sources)	

11	Interlaced video latency	
12	Interlaced audio latency (video delay for interlaced sources)	
13+	Additional bytes may be present, but the HDMI spec. says they shall be `00`.	

If a Speaker Allocation Data Block is present, it will consist of three bytes. The second and third are reserved (all `0`), but the first contains information about which speakers are present in the display device:

Speaker Allocation Data Block

Byte	**Description**	
0	Data block header	
1	1, present; `0`, absent:	
	Bit 7	Reserved, `0`
	Bit 6	Rear left and right center
	Bit 5	Front left and right center
	Bit 4	Rear center
	Bit 3	Rear left and right
	Bit 2	Front center
	Bit 1	Low-frequency effects (LFE)
	Bit 0	Front left and right
2–3	Reserved, `00 00`	

References

1. "CTA's Entire Library of Industry Standards Now Free to Everyone" (https://www.cta.tech/News/Press-Releases/2018/May/CTA-s-Entire-Library-of-Industry-Standards-Now-Fre.aspx). *www.cta.tech*. Retrieved 2 April 2020.
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16. see section 8.7 of HDMI 1.3a

External links

- edid-decode (https://git.linuxtv.org/edid-decode.git/) utility
- edidreader.com (http://www.edidreader.com/) – Web Based EDID Parser
- Edid Repository (https://github.com/linuxhw/EDID) – EDID files repository
- Display Industry Standards Archive (https://glenwing.github.io/docs/)